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EXAMINER
HUISMAN, DAVID J

ART UNIT	PAPER NUMBER
2183	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/598,558	Applicant(s) BARRY ET AL.
	Examiner David J. Huisman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☒ Claim(s) *6 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-13 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #3. Declaration as received on 10/26/2000, #4. Formal Drawings as received on 8/7/2000, #5. IDS as filed on 11/9/2000, #6. Change of Address/POA as received on 5/23/2001, #7. Change of Address/POA as received on 7/14/2001, and #8. Change of Address/POA as received on 8/29/2002.

Specification

3. The disclosure is objected to because of the following informalities: For all documents that are incorporated by reference, the application and/or patent number should be supplied along with the filing date. On page 8, line 12, should "PE/PEs" be replaced with --SP/PEs--? On page 8, line 19, replace "a" with --an--. On page 9, lines 16-17, it seems as if the 2nd paragraph is in an inappropriate position within the specification. Its placement is between the actual invention's description as opposed to being placed by the documents that are incorporated by reference. Please move this paragraph to a more appropriate position. On page 11, lines 6-6-8 are unclear to the examiner. It is specified that when no PE instructions are used, the core processor acts as a 1x0. However, according to Fig.3, when no PE instructions are used (S/P bit equals 0), the core processor acts as both a 1x1 (entry 320) and a 1x0 (entry 324), depending on the CSB bit. Finally, there is no mention of Fig.5B within the specification in the "Brief

Description of the Drawings" section. So, for instance, at the bottom of page 4, "Fig. 5" can be replaced with --Fig. 5A-B--.

Appropriate correction is required.

Drawings

4. The drawings are objected to because of the following minor informalities: In Fig.1, component 105 should be changed from "SP BIT" to --SP B-bit--. Furthermore, in Fig.1, Fig.4, and Fig.5A, should the C-bit instruction bus be changed to the B-bit instruction bus to match the memory size? In Fig.4, please change "C-BITINSTRUCION BUS" to --C-BIT INSTRUCTION BUS--. Also, in Fig.4, a closing parenthesis should be inserted after "PE0/1(PE00/01". A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 6 is objected to because of the following informalities: The wording of claim 6 is not clear to the examiner. More specifically, the phrase "...to determine which register files the SP's or the PE's are to be accessed for each instruction execution...". This phrase should be worded more appropriately.

6. Claim 8 is objected to because of the following informalities: Line 5 of claim 8 is ambiguous. It can either be interpreted as each PE having its own register file or that all of the PEs share a single second register file. It is recommended that the applicant reword the claim for

clarification. For purposes of this examination, this line will be interpreted as each PE has its own register file. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 2, 6-8, and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Lee et al., U.S. Patent No. 4,763,242 (as disclosed by applicant and herein referred to as Lee).

9. Referring to claim 1, Lee has taught apparatus comprising:

a) a first set of registers stored in a first register file. See Fig.1, component 119.

b) a second set of registers stored in a second register file. See Fig.3, component 339.

c) a sequence processor/processing element (SP/PE) selection bit in an instruction. See column 4, lines 48-54. Note that the processor field indicates whether the processing element 103 will be used or whether a sequence processor (assist processor) will be used.

d) a context select bit (CSB) in a processor state register which in conjunction with the SP/PE selection bit determines which set of registers is to be accessed by the instruction. See column 4, lines 66-68. Note that if the processor field of the instruction indicates that an assist processor will be used, the assist field then determines which sequence processor will execute the instruction. In this case either the SFU 107 or one of multiple coprocessors (COPs) 109 will perform the execution based on the content of the assist field. This field also determines which

register file will be used. For instance, each COP contains it's own register file. See Fig.3, component 339. If a COP instruction is encountered then the COP register file will be used while the COP is executing the instruction. On the other hand, if the main processor is executing the instruction, then its register file 119 will be accessed. Therefore, a register context is selected by the assist field of the instruction.

10. Referring to claim 2, Lee has taught apparatus as described in claim 1. Lee has further taught that the first register file is a sequence processor register file and the second register file is a processing element register file. From Fig.1 and Fig.3, since the processing element 103 and COP 109 have their own register files 119 and 339, then the register files can be considered a processing element register file and a sequence processor register file, respectively.

11. Referring to claim 6, Lee has taught apparatus as described in claim 1. Lee has further taught that the SP/PE selection bit is used in a 1x1 array core having SP register files and PE register files to determine which register files the SP's or the PE's are to be accessed for each instruction execution when the CSB is inactive and to have both SP and PE instructions use the PE register files when the CSB is active. Recall from the rejection of claim 1 that the assist field of an instruction is interpreted as performing the same function as the CSB bit. When the assist field is inactive, i.e., if a non-basic instruction is encountered and the assist field must be used to map the instruction to a specific coprocessor (COP), then the selected register file will be the register file associated with the selected COP. This is because each COP has its own register file, as shown in Fig.3. On the other hand, if the assist field is active, i.e., if a non-basic instruction is encountered and the instruction must be mapped to a specific special function unit (SFU), then the selected register file will be the main processor's (PE) register file. See column

2, lines 57-58. Therefore, it can be seen that both SP and PE instructions would use the PE's register file when the assist field (CSB) is active (note that all basic instructions use the PE's register file - column 4, lines 49-54).

12. Referring to claim 7, Lee has taught apparatus as described in claim 1. Lee has further taught that the first or second register files may comprise reconfigurable compute register files (CRF), address register files (ARF), miscellaneous register files (MRF) or a combination of CRF, ARF and MRF files. Note that the first register file 119 contains registers (CRF) used for basic operations (column 4, lines 48-54) and that register file 119 also includes address registers (ARF) which store the addresses of assist instructions and coprocessor configuration registers (MRF). See column 7, lines 1-23.

13. Referring to claim 8, Lee has taught apparatus for providing efficient context switching between tasks in a manifold array (ManArray) multiple processor environment in which a sequence processor (SP) and multiple processing elements (PE) are employed, said apparatus comprising:

a) a first set of registers stored in a first register file for the SP. See Fig.1, component 119.

b) a second set of registers stored in a second register file for each of the PEs. See Fig.3, component 339. Also, note that a plurality of COPs could exist (as shown in Fig.3), each having its own register file.

c) a sequence processor/processing element (SP/PE) selection bit in an instruction. See column 4, lines 48-54. Note that the processor field indicates whether the sequence processor 103 will be used or whether a processing element (assist processor) will be used.

d) a software controllable context select bit (CSB) in a processor state register which in a logical combination with the SP/PE selection bit reconfigures the ManArray by selecting a first context in which the ManArray is configured in a first configuration or a second context in which the ManArray is configured in a second configuration. See column 4, lines 66-68. Note that if the processor field of the instruction indicates that an assist processor will be used, the assist field then determines which processing element will execute the instruction. In this case either the SFU 107 or COP 109 will perform the execution based on the content of the assist field. This field also determines which register file will be used. For instance, the COP contains it's own register file. See Fig.3, component 339. If a COP instruction is encountered then the COP register file will be used while the COP is executing the instruction. On the other hand, if the main processor is executing the instruction, then its register file 119 will be accessed. Therefore, a register context is selected by the assist field of the instruction.

14. Referring to claim 11, Lee has taught a method for providing efficient context switching in a manifold array processor having a sequence processor and multiple processing elements, the method comprising:

a) setting a sequence processor/processing element (SP/PE) selection bit in an instruction. See column 4, lines 48-54. Note that the processor field indicates whether the sequence processor 103 will be used or whether a processing element (assist processor) will be used.

b) setting a context select bit (CSB). See column 4, lines 66-68. Note that if the processor field of the instruction indicates that an assist processor will be used, the assist field (CSB) then determines which processing element will execute the instruction.

c) utilizing the SP/PE selection bit in conjunction with the context select bit to determine a context for operation. These bits determine which register file will be used. For instance, the COP contains its own register file. See Fig.3, component 339. If a COP instruction is encountered then the COP register file will be used while the COP is executing the instruction. On the other hand, if the main processor is executing the instruction, then its register file 119 will be accessed. Therefore, a register context is selected by the processor field (SP/PE bit) and assist field (CSB) of the instruction.

d) configuring the manifold array processing depending upon the context. Through the different values of the processor field and assist field of an instruction, an array of COPs (multiple COPs) can be configured to execute instructions, each one having its own register file and therefore, each having its own context.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 3-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, as applied above, in view of Dowling, U.S. Patent No. 6,128,728.

17. Referring to claim 3, Lee has taught apparatus as described in claim 1. Lee has not explicitly taught means for allowing the first set of registers to be saved and restored from memory in the background while a task is using the second set of registers in the foreground; and for allowing the second set of registers to be saved and restored from memory in the background

while a task is using the first set of registers in the foreground. However, Dowling has taught such a concept. See column 4, lines 32-46, and column 5, line 14, to column 6, line 6. With such a scheme, the inactive register set can be loaded and stored in the background while the active register set can be manipulated by the processor in the foreground. This would maximize the efficiency by making use of otherwise unused external memory cycles, as disclosed in the abstract. That is, when the processor is not accessing memory, the inactive register set can be loaded or stored in the background during those unused memory cycles. Therefore, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to save and restore a second register set from memory in the background while a task is using a first register set in the foreground.

18. Referring to claim 4, Lee in view of Dowling has taught apparatus as described in claim 3. Dowling has further taught that said means for allowing comprises a pair of background address registers to provide store and load addresses. See Fig.7, components 780 and 790. Also, for a brief description, see column 19, lines 2-23 (it has been noted that the reference numbers of the specification do not match all of the numbers in Fig.7, but this should be recognized by one of ordinary skill in the art).

19. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee, as applied above, in view of Dowling, U.S. Patent No. 6,170,051 (herein referred to as Dowling2).

20. Referring to claim 5, Lee has taught apparatus as described in claim 1. Lee has further taught a plurality of execution units (see Fig.1, components 145, 117, and 137, for instance) but has not explicitly taught a multiplexer connected to select which registers the execution units

read data from and write data to, the multiplexer controlled by a logical combination of the SP/PE selection bit and the CSB. However, Dowling has taught such a concept. See Fig.3, component 320. A person of ordinary skill in the art would have recognized that within Lee's system, only a single register file can be accessed for a particular instruction, and this register file is determined by the SP/PE (processor field) and CSB (assist field). Therefore, since a multiplexer provides a means for selecting between multiple sources (in this case, register files), then it would have been obvious to one of ordinary skill in the art at the time of the invention to use a multiplexer to control access to a particular register file based on the SP/PE and CSB bits.

21. Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dahl et al., U.S. Patent No. 5,710,938 (herein referred to as Dahl), in view of Lee, as applied above.

22. Referring to claim 8, Dahl has taught an array multiple processor environment in which a sequence processor (SP) and multiple processing elements (PE) are employed (see Fig.1, components 21 and 12). Dahl has not taught that the array environment includes apparatus for providing efficient context switching between tasks. However Lee has taught such an apparatus, comprising:

a) a first set of registers stored in a first register file for the SP. See Fig.1, component 119.

b) a second set of registers stored in a second register file for each of the PEs. See Fig.3, component 339. Also, note that a plurality of COPs could exist (as shown in Fig.3), each having its own register file.

c) a sequence processor/processing element (SP/PE) selection bit in an instruction. See column 4, lines 48-54. Note that the processor field indicates whether the sequence processor 103 will be used or whether a processing element (assist processor) will be used.

d) a software controllable context select bit (CSB) in a processor state register which in a logical combination with the SP/PE selection bit reconfigures the ManArray by selecting a first context in which the ManArray is configured in a first configuration or a second context in which the ManArray is configured in a second configuration. See column 4, lines 66-68. Note that if the processor field of the instruction indicates that an assist processor will be used, the assist field then determines which processing element will execute the instruction. In this case either the SFU 107 or COP 109 will perform the execution based on the content of the assist field. This field also determines which register file will be used. For instance, the COP contains it's own register file. See Fig.3, component 339. If a COP instruction is encountered then the COP register file will be used while the COP is executing the instruction. On the other hand, if the main processor is executing the instruction, then its register file 119 will be accessed. Therefore, a register context is selected by the assist field of the instruction.

A person of ordinary skill in the art would have recognized that by implementing the concept of context switching within Dahl's system, Dahl could assign different tasks to different processing elements, where each task deals with its own register file contents (note that each task has its own context so in essence, as fetched instructions signify a new task, the context is switched). This allows for an instruction set extension, as disclosed in the abstract, which may allow for increased functionality. Context switching also allows for the executing a second task when a first task is idle for instance. Therefore, in order to increase efficiency, it would have been

obvious to one of ordinary skill in the art at the time of the invention to provide an apparatus for context switching (as described in Lee) in the array-processing environment of Dahl.

23. Referring to claim 9, Dahl in view of Lee has taught apparatus as described in claim 8. Dahl has not explicitly taught that the ManArray is a 1x2 array and said first configuration is a 1x2 and said second configuration is a 1x1. However, Dahl has taught the general concept of reconfiguring an array into subarrays. See column 1, lines 42-51. This is desirable because each subarray could load and run separate applications without interaction with other subarrays. This, in turn, would greatly increase the usefulness of the overall array. Although Dahl has not explicitly disclosed the dimensions of the array, a change in size/range is not generally given patentable weight or it would have been considered an obvious improvement. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a 1x2 ManArray where the first configuration in a 1x2 and the second configuration is a 1x1.

24. Referring to claim 10, Dahl in view of Lee has taught apparatus as described in claim 8. Dahl has not explicitly taught that the ManArray is a 1x5 array and said first configuration is a 1x5 and said second configuration is a 2x2. However, Dahl has taught the general concept of reconfiguring an array into subarrays. See column 1, lines 42-51. This is desirable because each subarray could load and run separate applications without interaction with other subarrays. This, in turn, would greatly increase the usefulness of the overall array. Although Dahl has not explicitly disclosed the dimensions of the array, a change in size/range is not generally given patentable weight or it would have been considered an obvious improvement. As a result, it would have been obvious to one of ordinary skill in the art at the time of the invention to have a 1x5 ManArray where the first configuration in a 1x5 and the second configuration is a 2x2.

25. Referring to claim 11, Dahl has taught an array processor having a sequence processor and multiple processing elements. Dahl has not taught a method for providing efficient context switching in the array processor. However Lee has taught:

a) setting a sequence processor/processing element (SP/PE) selection bit in an instruction. See column 4, lines 48-54. Note that the processor field indicates whether the sequence processor 103 will be used or whether a processing element (assist processor) will be used.

b) setting a context select bit (CSB). See column 4, lines 66-68. Note that if the processor field of the instruction indicates that an assist processor will be used, the assist field (CSB) then determines which processing element will execute the instruction.

c) utilizing the SP/PE selection bit in conjunction with the context select bit to determine a context for operation. These bits determine which register file will be used. For instance, the COP contains its own register file. See Fig.3, component 339. If a COP instruction is encountered then the COP register file will be used while the COP is executing the instruction. On the other hand, if the main processor is executing the instruction, then its register file 119 will be accessed. Therefore, a register context is selected by the processor field (SP/PE bit) and assist field (CSB) of the instruction.

d) configuring the manifold array processing depending upon the context. Through the different values of the processor field and assist field of an instruction, an array of COPs (multiple COPs) can be configured to execute instructions, each one having its own register file and therefore, each having its own context.

A person of ordinary skill in the art would have recognized that by implementing the concept of context switching within Dahl's system, Dahl could assign different tasks to different processing

elements, where each task deals with its own register file contents (note that each task has its own context so in essence, as fetched instructions signify a new task, the context is switched). This allows for an instruction set extension, as disclosed in the abstract, which may allow for increased functionality. Context switching also allows for the executing a second task when a first task is idle for instance. Therefore, in order to increase efficiency, it would have been obvious to one of ordinary skill in the art at the time of the invention to provide an apparatus for context switching (as described in Lee) in the array-processing environment of Dahl.

26. Claims 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dahl in view of Lee, as applied above, and further in view of Mirsky et al., U.S. Patent No. 5,915,123 (herein referred to as Mirsky).

27. Referring to claim 12, Dahl in view of Lee has taught a method as described in claim 11.

a) Dahl in view of Lee has not taught identifying each PE with both a virtual identifier and a physical identifier. However, Mirsky has taught such a concept. See column 7, lines 29-53 and the abstract. A physical identification allows for the selection of individual processing elements while the virtual identification allows for the selection of one or more processing elements based on a programmable identifier, allowing the software to design its own address space. These different options result in increased flexibility for the programmer. See column 8, lines 6-18. Therefore, in order to increase programmer flexibility, it would have been obvious to one of ordinary skill in the art at the time of the invention to identifying each PE with both a virtual identifier and a physical identifier, as taught by Mirsky.

b) Dahl in view of Lee has not taught identifying each PE utilizing its physical identifier in a first context and identifying each PE utilizing its virtual identifier in a second context. However, Mirsky has shown that data transmitted to the processing elements is used in selecting whether the physical or virtual identification is used. See column 13, lines 27-30, and column 7, lines 47-53. From this it can be seen that each PE can be identified using its physical identifier in a first context (if the transmitted data associated with the first context specifies physical identification) and each PE can be identified using its virtual identifier in a second context (if the transmitted data associated with the second context specifies virtual identification). With this scheme, each context can identify PEs in a way that is most convenient for that context. For instance, virtual identification may be best for the second context if that context requires the selection of multiple PEs, while if the first context only requires one PE, then physical identification would suffice. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to identify each PE utilizing its physical identifier in a first context and identify each PE utilizing its virtual identifier in a second context.

28. Referring to claim 13, Dahl in view of Lee and further in view of Mirsky has taught a method as described in claim 12. Lee has further taught that the first context is when the CSB bit is inactive and the second context is when the CSB bit is active. Recall from the rejection of claim 11 that the assist field of an instruction is interpreted as performing the same function as the CSB bit. When the assist field is inactive, i.e., if a non-basic instruction is encountered and the assist field must be used to map the instruction to a specific coprocessor (COP), then the selected register file will be the register file associated with the selected COP. This is because each COP has its own register file (context), as shown in Fig.3. On the other hand, if the assist

field is active, i.e., if a non-basic instruction is encountered and the instruction must be mapped to a specific special function unit (SFU), then the selected register file will be the main processor's (PE) register file. See column 2, lines 57-58. Therefore, it can be seen that when the CSB allows for a first context, within the COP, when it is inactive, and a second context, within the main processor, when it is active.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Hammond et al., U.S. Patent No. 6,209,085, has taught a method and apparatus for performing process switching in multiprocessor computer systems. Hammond has taught a system wherein the context switches result in a minimal amount of data copied to/from register files.

Panwar et al., U.S. Patent No. 5,890,008, has taught a method for dynamically reconfiguring a processor. More specifically, the amount of processing elements is configured based on the amount of threads created.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
June 5, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100